

CLAIMS

What is claimed is:

- SUB B1 7
1. An integrated circuit comprising
NMOS transistors in P-wells,
PMOS transistors in N-wells, and
at least one PNP bipolar transistor having
5 an emitter diffusion which has a doping profile which combines
said P-wells with P+ source diffusions of said PMOS
transistors, and
a base diffusion which at least partly underlies said emitter
diffusion, and which has a doping profile which is at least
10 partly the said as said N-wells;
said emitter and base diffusions jointly defining an emitter:base
ratio of near-junction dopants, measured at 75% and 125%
of the emitter-base junction depth, which is greater than
two to one.
2. The integrated circuit of Claim 1, 4, 7, wherein said emitter
diffusion further comprises a P+ diffusion which is also
implanted into the sources of said PMOS transistors.
- SUB B2 7
3. The integrated circuit of Claim 1, 4, 7, further comprising a blanket
P-type diffusion component having a peak concentration depth
more than twice that of said p-well.

4. An integrated circuit comprising

NMOS and PMOS transistors, and

a PNP bipolar transistor which includes

a P-type emitter diffusion, having at least one implanted
diffusion profile which is the same as at least one
implanted diffusion component of p-wells which contain at
least some of said NMOS transistors;

an N-type base diffusion, having at least one implanted diffusion
profile which is the same as at least one diffusion
component of n-wells which contain at least some of said
PMOS transistors;

wherein the peak of said p well is no deeper than the peak of said
n well.

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5. The integrated circuit of Claim 1, 4, 7, wherein said emitter
diffusion further comprises a P+ diffusion which is also
implanted into the sources of said PMOS transistors.

6. The integrated circuit of Claim 1, 4, 7, further comprising a blanket
P-type diffusion component having a peak concentration depth
more than twice that of said p-well.

9. An integrated circuit fabrication method, comprising the steps of:
- (a) implanting p-type dopants into p-well locations and PNP emitter locations, but not into all locations;
 - (b) implanting n-type dopants into n-well locations and PNP emitter locations, but not into all locations;
 - (c) implanting p-type dopants into PMOS source/drain locations and PNP emitter locations, with a stopping distance less than half of that used in said step (a); and
 - (d) implanting p-type dopants overall, with a stopping distance more than twice that used in said step (c);
- whereby emitter efficiency of resulting PNP transistors is improved.